Error Types in SDRAMS

M. Shoga
The Radiation Group, Inc.
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ABSTRACT

This paper describes single event effects (SEE) error types observed testing SDRAMs. Visual maps of these error types are shown in this paper. Such error maps enhances the understanding and thus handling the error types in the system. Better event rates can be calculated from understanding the errors observed in a memory map. Some of these error types cannot be protected with simple error detection and correction (EDAC) codes and requires sophisticated schemes.

Post irradiation data analysis includes identifying the characteristics of single upsets due to ion hits to memory array, multiple upsets, pattern upsets, column and row upsets, block upsets, and total memory upsets. With proper testing, one can differentiate hits to the cell array from hits to control logic circuitry.

BACKGROUND:

Various SDRAM sizes (64M, 128M, and 256M, 512M, and 1GB) from various vendors were tested using an automated test system designed specifically for SEU testing memory parts. The system is capable of storing the errors and their addresses.

SDRAMs were tested using different patterns, all 0's, all 1's, checkerboard, inverse checkerboard, count, inverse count, general purpose, and random patterns. They were tested in all modes, namely, self-refresh, auto refresh, read, write, no op, etc. Data files were analyzed using a visual error map software. Data analysis involves identifying error types including, singles, multiples, patterns, functional interrupts (SEFI), and latchups.

TEST RESULTS

For each run, the errors were visually displayed. The software tool has the capability to search for ordered and arbitrary patterns of errors. Figure 1 displays a sample result of a 256MB SDRAM.

In this case, the memory array is represented by four main blocks; Block 0, 1, 2, and 3 (top section of Figure 1). Each block contains 64 x 4 cells; each cell consists of 32 rows (middle section of Figure 1); each row consists of 2048 columns (bottom

section of Figure 1); and each column represents a nibble (four bits). The observed error types are as follows:

Individual errors (SEUs):

This type of upset is the result of a direct hit to an individual cell inducing a single even upset (SEU).

Column-Pattern Errors:

This is the result of a hit to a gate or a register in the control logic circuitry. Figure 1 shows a 3-column error pattern (3 red cells in Bank 0) which corresponds to the white square of a magenta row (top figure). A search on this pattern identified a repeated occurrence of 767 times (Bank 0, magenta color with black dots, shows all the locations of this type of error).

Figure 1. 3-column errors repeated in 767 rows

Arbitrary-Pattern Errors:

This is the result of a hit to a gate or a register in the control logic circuitry. Figure 2 shows an arbitrary pattern of 21 errors (marked red in the lower section). The search for this pattern identified a repeated occurrence of many times. Figure 2, top

section, red color with black dots in Bank 0, shows all the locations of this type of error (bottom map).

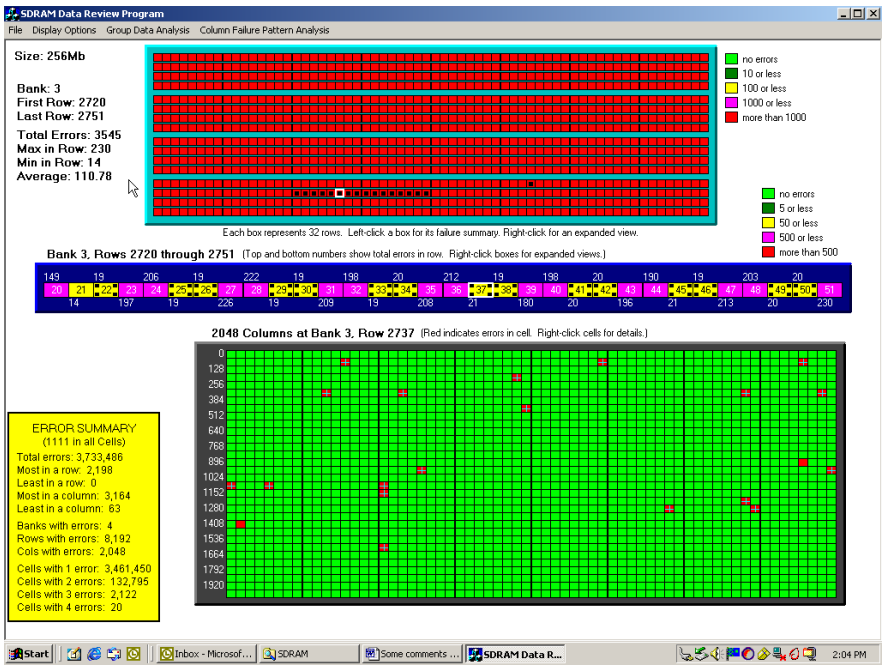

Figure 2. Arbitrary 21-column errors repeated in 20 rows

Half-Row upset patterns:

This is the result of a hit to a gate or register in the control logic circuitry. Figure 3 (lower section) shows top-half row error; this error pattern is repeated 10 times, as shown, cells in red color with dark dots (top section of figure 3).

Figure 3. One half (top) row upset pattern

Full-Row upset patterns:

This is the result of a hit to a gate or a register in the control logic circuitry. This figure is not shown here. A full-row error pattern upsets repeated through out one half Block 0 only, a total of 5196 rows got upset with one ion hit.

Total-Memory upset patterns:

This is the result of a hit to a gate or a register in the control logic circuitry. When software reset was applied, only portion of the memory was recovered. Block 0 did not recover; top-half row error type remained upset in Block 0 cells (will be shown in full paper).

Latch up Errors:

(Figure will be shown in the full paper). A 128MB SDRAM showing latch up at LET of 45, all memory cells were in upset state. The supply current increased and remained high (256 mAmp). The part did not respond to software reset. The part only recoved after power reset was applied.

CONCLUSION:

Various types of errors occur in SDRAMs. Large number of errors represents patterns of upsets that may or may not be correctable with ECC codes. There is certain dependency of error types on the mode of operation of the SDRAM. An

application-upset rate is dependent on the modes of operation and on the duty cycles of such mode.